2022 37th International Technical Conference on Circuits/Systems, Computers and Communications (ITC-CSCC) | 978-1-6654-8559-3/22/$31.00 ©2022 IEEE | DOI: 10.1109/ITC-CSCC55581.2022.9894896

Idle period frequency scaling to reduce dynamic power of display driver IC

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***Abstract*—The proportion of power consumption occupied by the display panel in the mobile device is increasing due to the driving the high frame rate and the increase in resolution. Among them, the power of the display driver IC (DDI), a core component that drives the display panel, was also increased. Recently, Variable Refresh Rate (VRR) technology has been widely used to reduce display panel power consumption, and to this end, DDI is also equipped with technology for VRR driving. During VRR operation, DDI can operate at a low frame rate, which is possible by extending the DDI idle period. During the idle period extension, dynamic power is still flowing because the clock is still toggling in the idle period. This paper introduces a frequency scaling technique through internal clock dividing in the idle period during the VRR operation. As a result of the frequency scaling we propose, at a sampling frame rate less than 60Hz, the power-saving effect of 8.82% on average and 11.11% on maximum can be confirmed through power simulation.**

***Index Terms*—Display driver IC, Variable Refresh Rate, Frequency scaling, Idle period, Porch period.**

I. Introduction

Variable Refresh Rate (VRR) [1] technology is widely used to reduce mobile devices, especially display panel power consumption. VRR is a technology that detects still images when the mobile device is operating in a normal mode such as 120Hz or 60Hz, automatically lowers the frame rate properly, and conversely, increases the frame rate when an image update event occurs. The frame rate is controlled through display driver IC (DDI), and when the DDI checks the presence or absence of image update and confirms entry from the application processor (AP) to Panel Self-Refresh mode (PSR) [2], it is recognized as a still image and is controlled by a low frame rate. The most common way for DDI to control the low frame rate is to extend the porch period, which is an idle period, except for the active period that processes the image at a fixed time of DDI. When the DDI and display panels reach a low frame rate, the overall power consumption decreases, but from the DDI's point of view, additional dynamic power occurs as the internal clock continues to toggle during the porch period. Although clock gating is applied to DDI internal circuits as much as possible, switching power flowing from the entire clock network cannot be ignored because the porch period increases toward the low frame rate. The best way to reduce dynamic power is frequency scaling. However, during the active period, DDI must process images at a predetermined frame time. So, if we scale down the clock frequency, the number of clocks for processing images can be insufficient. Also, Electromagnetic Interference (EMI) can be occurred between mobile device communication frequency and DDI clock frequency. In conclusion, there is a limitation in that the speed of the DDI clock source cannot be freely adjusted.

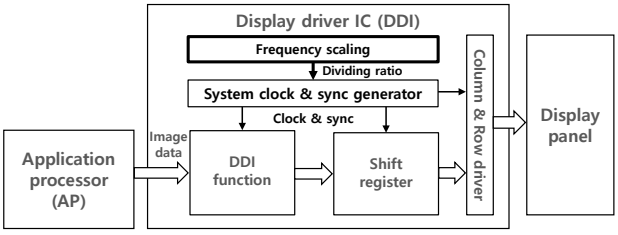

Fig. 1. Proposed DDI frequency scaling

We introduce a porch period frequency scaling technique using an internal clock dividing technique rather than an external clock source scaling approach to reduce dynamic power consumption while overcoming limitations.

Fig. 1 is a block diagram of the DDI frequency scaling we want to propose. The Frequency scaling block classifies the porch period, excluding the active period

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that processes the image data received from the AP and transfers the internal clock dividing ratio value to the clock & sync generator. The internal system clock is divided and operated during the porch period with the received dividing ratio value. In the case of the active period, image data must be processed within a set time. So, if the clock dividing scheme is applied, it can cause a lack of clocks to process image data during line time.

II. Background

DDI controls image data and panel-related signals so that the display panel can always display the image at a constant frame rate. Because it is necessary to maintain a constant frame rate, the image processing cycle is always constant.

Fig. 2 is a summary of the DDI basic control system. DDI processes frame rate control and image with VSYNC, a Vertical Sync flag, and HSYNC, a Horizontal Sync flag. The time between VSYNC is defined as frame time, which is determined by the frame rate.

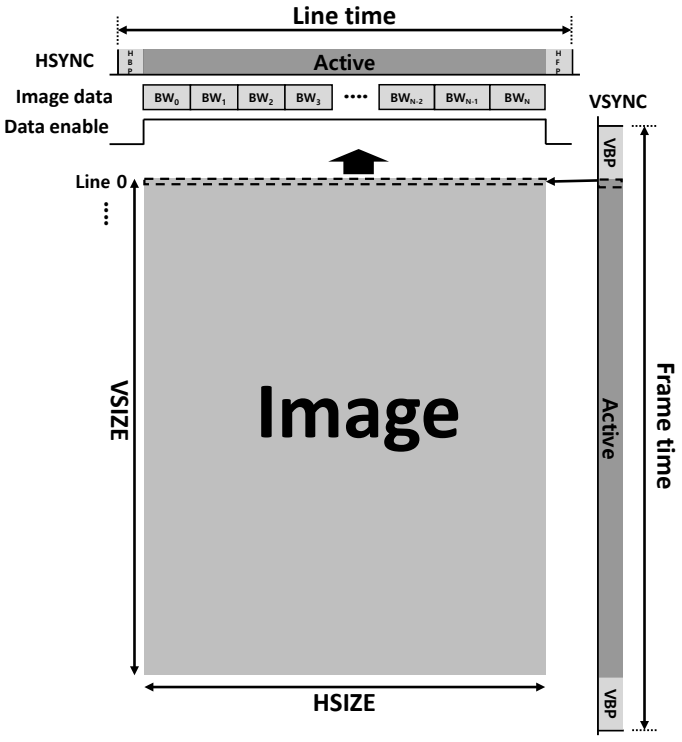

Fig. 2. DDI basic control scheme

The image is processed at a set time in a frame time, and a frame time is divided into an active period, a porch period between VSYNC, and the image is processed line by line, which is the time between HSYNC. Within frame time and line time, the porch period is divided into VSYNC front and back Vertical Front Porch (VFP) and Vertical Back Porch (VBP) and HSYNC front and back Horizontal Front Porch (HFP) and Horizontal Back Porch (HBP). Between frame times, there is currently a line time of vertical image size (VSIZE), VBP, and VFP, and one line time consists of image pixel data processing time of horizontal image size (HSIZE) and HFP, HBP exists.

The most widely used method of adjusting the frame rate in DDI is to extend the VFP section. According to the image resolution and the currently determined frame rate, the number of line times is determined within a constant frame time.

As shown in Fig. 1, the display panel is controlled by the column and row driver of DDI, where one horizontal line data is controlled at once for image data. Since one horizontal line data is processed at once, it is put in the shift register every line time and loaded to the panel display line by line. The shift register for image processing in DDI is usually divided into left and right, and each processes half of the image.

III. Idle Period Frequency Scaling

Fig. 3 is the timing diagram for the DDI frequency scaling during the porch period, which is an idle period, we propose. Separate the active period that processes image data from the frequency scaling module described in Fig. 1 and deliver the dividing ratio to the clock and sync generator when entering the frequency scaling module.

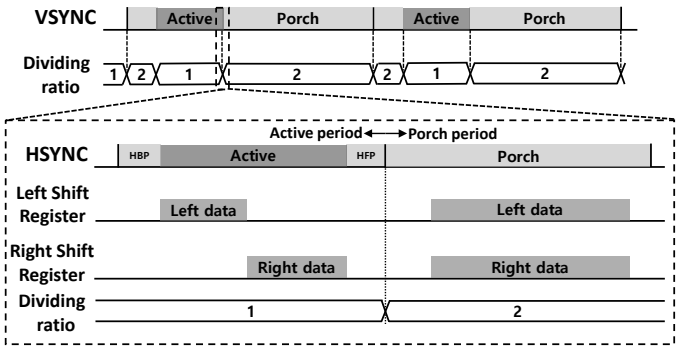

Fig. 3. Porch period frequency scaling

The active period and the porch period are divided within the frame time by receiving the resolution of image data input through the AP in the frequency scaling module and the number of VFP and VBP lines set for the current frame rate. The clock and sync generator module that has received the dividing ratio proceeds with the internal clock dividing from the first HSYNC after entering the porch period. Image data processing

does not occur during the porch period, but to minimize leakage of display panel cells, image last line data is continuously uploaded to the display panel through the shift register during every line time.

Because of these reasons, both left and right shift registers must be operated. But the number of clocks that can operate the shift register is insufficient because the clock is divided, so the left and right shift register cannot be operated serially like the active period.

Therefore, as shown in Fig. 3, this problem is solved by simultaneously processing the left and right shift registers in parallel. Even if it is processed in parallel, the line time does not change, so in this paper, simulation is conducted by limiting the maximum dividing ratio to a 2-dividing ratio. Since the last line of image data is already captured in the shift register, only the clock is toggled to refresh and deliver it to the display panel, there is no problem with processing the left and right shift register in parallel, and it is not a visible area.

Due to the characteristic of DDI, image data is transmitted from AP and stored in Graphic memory (GRAM) inside the DDI, and in the image update frame, which also writes images at the porch period, the performance is limited when the clock speed slows.

Therefore, frequency scaling cannot be performed in the image update frame. As shown in Fig. 4, frequency scaling is stopped in the image update frame, and frequency scaling is performed in the Self-refresh frame that operates by calling up the image stored in the GRAM without image update.

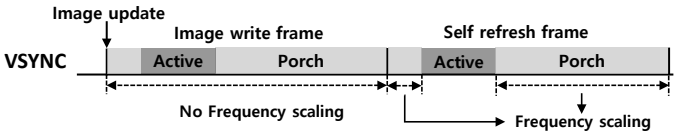

Fig. 4. Proposed DDI frequency scaling sequence

As mentioned in the introduction section, the DDI low frame rate is controlled by extending the porch period, especially the VFP section, as shown in Fig. 5. So, because our frequency scaling technique is applied to the porch period, we can expect that the power saving effect increases as DDI goes to the low frame rate.

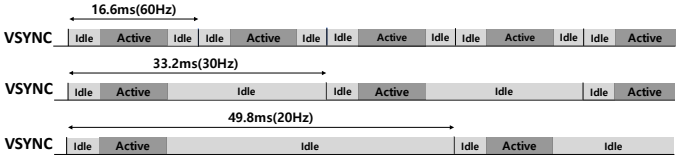

Fig. 5. DDI frame rate control example

IV. Experiment setup

To simulate the power saving effect of the proposed frequency scaling, we extract active period and porch period dynamic power through Synopsys PrimeTime PX [3] with a post netlist of benchmark DDI. We conduct our experiments with how much porch period dynamic power saving accounts for the total dynamic power saving based on the extracted information.

For frame rate, including the default of 60Hz, the most used low frame rate in DDI is selected as the sampling frame rate, which is equivalent to 30Hz, 15Hz, 10Hz, 5Hz, and 1Hz.

The experiment is conducted with three categories of messenger, movie, and App main image, which are the most frequently used screens while using mobile phones, as well as white, which is a monochromatic pattern, and finally, checkerboard pattern, which is the worst pixel toggling pattern. More detailed simulation conditions are described in TABLE I.

TABLE I. Simulation environment

Experiment condition	Description
Benchmark IC	Samsung galaxy model display driver IC
Resolution	1440Hx3200V(WQHD+)
Clock speed	169.9Mhz
Frame rate	60Hz(default), 30Hz, 15Hz, 10Hz, 5Hz, 1Hz
Power simulation tool	Synopsys PrimeTime PX
Test images	5-categories(Messenger, White pattern, 4x1 checkerboard, Movie, App main)

V. Experimental results

As shown in Fig. 6, we obtain the dynamic power saving rate for each category image when applying the frequency scaling in the porch period, which we propose at 60Hz, 30Hz, 15Hz, 10Hz, 5Hz, and 1Hz sampling frame rates.

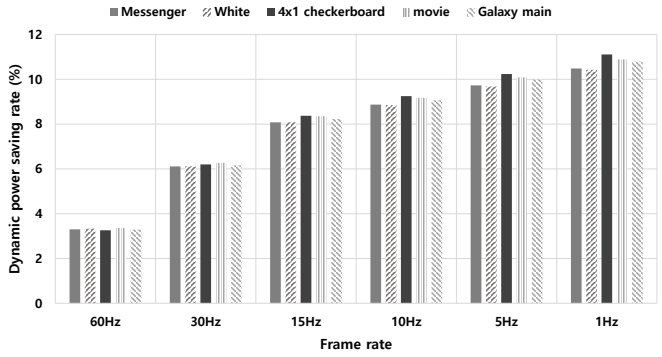

Fig. 6. Simulation results

As a result, compared with the dynamic power of no frequency scaling in the porch period, a power-saving rate result of an average of 8.82% of the total frame rate is obtained except for 60Hz, which is the default frame rate, and a power-saving rate result up to 11.11% is obtained at 1Hz. The power-saving rate is slightly different for each image category because the power in the porch period is affected to a certain extent by the image pattern processed in the active period, but not that much.

VI. Conclusion

This paper obtains up to 11.11% dynamic power saving results due to the proposed DDI idle period frequency scaling compared with the dynamic power of the no frequency scaling case. For future work, we will study frequency scaling techniques applicable to the active period based on our current results.

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